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2124 #2 BT 5-10-02

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: : Atty. Docket No.: 01-LJ-062
Sivagnanam PARTHASARATHY et al. : Group Art Unit: 2124
Serial No.: 10/032,742 :
Filed: October 22, 2001 :
For: FLEXIBLE GALOIS FIELD MULTIPLIER :

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D. C. 20231

Sir:

The attached Form PTO-1449 provides a listing of information which may be relevant to the subject application. This IDS is not intended as a representation that better art is not available, nor that the information provided is prior art.

This IDS is submitted under:
__XX__ 37 CFR 1.97(b) - No Fee.
____ 37 CFR 1.97(c) - No Fee, with Certification.
____ 37 CFR 1.97(c) - Fee.
____ 37 CFR 1.97(d) - Fee, Certification & Petition.

The Commissioner is authorized to charge any required fees under 37 CFR 1.17(p) and (i) (1) to Deposit Account No. **50-1556.**

Respectfully submitted,

Date: 4/16/02

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Form PTO-1449 U.S. Dept. of Commerce Patent & Trademark Office List of Documents Cited by Applicant (Use several sheets if necessary)	Atty. Docket: 01-LJ-062	Serial No. 10/032,742
	Applicant: Sivagnanam PARTHASARATHY et al.	
	Filing Date: October 22, 2001	Group Art Unit: 2124

U.S. PATENT DOCUMENTS

Ex'rs Int'l		Document Number	Date	Name	Class	Sub-class	Filing Date, if applicable

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Sub-class	Transl'n Yes/No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AA1	Reed Solomon Decoder: TMS320C64x Implementation; Application Report, SPRA686, December 2000.
	AA2	Hasan, M.A. "An Architecture for a Universal Reed-Solomon Encoder using a Triangular Basis Multiplication Algorithm", IEEE CCECE/CCGEI, 1993, pp. 255-258.
	AA3	Hasan, M.A. et al. "Efficient Architectures for Computations Over Variable Dimensional Galois Fields", IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 45, No. 11, November 1998, pp. 1205-1211.
	AA4	Wicker, S.B. et al. "Reed-Solomon Codes and Their Applications", IEEE Press, pp. 68-70.
	AA5	Furness, R. et al. "Multiplication Using the Triangular Basis Representation Over GF(2^m)", 1996 IEEE, pp. 788-792.
	AA6	Furness, R. et al. "Generalised Triangular Basis Multipliers for the Design of Reed-Solomon Codecs", 1997 IEEE, pp. 202-211.
	AA7	Paar, C. "Efficient VLSI Architectures for Bit Parallel Computation in Galois Fields", PhD Thesis, University of Essen, June 1994, Chapter 5, pp. 42-58.
	AA8	Paar, C. et al. "Efficient Multiplier Architectures for Galois Fields GF(2^{4n})", IEEE Transactions on Computers, Vol. 47, No. 2, February 1998, pp. 162-170.
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Examiner:	Date Considered:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.